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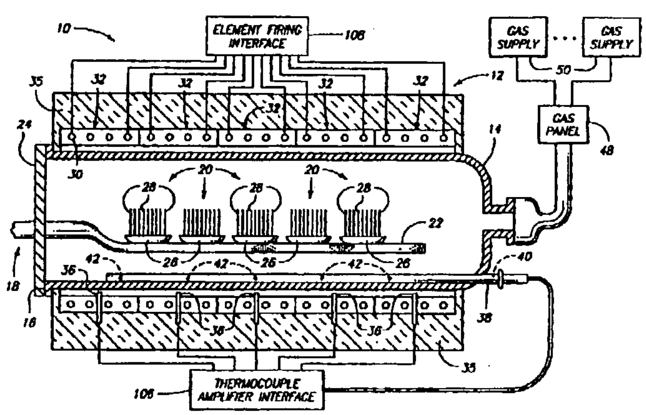

(57) Abstract

Controllers and associated methods for controlling a thermal reactor or other thermal semiconductor processors which include a heating element (30) powered by a power source, and having profile thermocouples (42) and spike thermocouples (36). One preferred method comprises the following steps: modeling thermal dynamic characteristics of the thermal reactor (12), the modeling step including providing thermocouple instrumented wafers (26) in the thermal reactor, perturbing the thermal reactor by controlling the heating element (30) using a stimulation sequence, and developing models based on changes in temperature created by the perturbations. The models are developed off-line and can include one or more models, such as a model of power versus spike thermocouple readings, a model of spike thermocouple reading versus profile thermocouple readings, and a model of profile thermocouple readings versus thermocouple instrumented wafer readings. On-line models are further derived and used during operation to control power input to the zones of the thermal processor using measured profile and spike temperatures. The models can be cascaded or selectively activated to achieve different control regimes.

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Model Based Temperature Controller For Semiconductor Thermal Processors

TECHNICAL FIELD

The invention relates to semiconductor processing methods and apparatus. More particularly, the invention relates to process controllers principally for controlling temperature and possibly other process variables in thermal reactors and other processors used in semiconductor processing.

BACKGROUND OF THE INVENTION

The processing of semiconductor wafers has become of great economic significance due to the large volume of integrated circuits being produced and the significant value associated with such circuits. Competitive pressures have driven dramatic changes in production. Foremost among these is the reduction in size of the various features of an integrated circuit which make up the transistors and other devices being formed on the integrated circuits. This reduction in feature size has been driven to achieve greater levels of integration, more sophisticated and complex circuits, and to reduce production costs by obtaining more integrated circuits on each wafer being produced.

Even though feature sizes used in integrated circuits have decreased dramatically, additional reductions are continuously being pursued. The temperature at which wafers are processed has a first order effect on the diffusion of dopants,

deposition of materials or other thermal processes being performed. Thus it is important to have processing equipment which can achieve accurate temperature control to meet desired thermal processing specifications. As feature size decreases, the importance of accurate temperature control during processing increases to even a greater degree.

Traditionally, semiconductor thermal reactors have used Proportional-Integral-Derivative (PID) controllers to control temperature. Although such controller have the advantage of easier operation and maintenance, they are of limited accuracy in controlling temperatures. This limited accuracy imposes limitations on the achievable size and yield of integrated circuits.

The more typical PID controller parameters are experimentally tuned by adjusting the gain values or selected using a variety of tuning rules (e.g., Ziegler-Nichols). Such control methods give relatively less accurate control of the temperature of the thermal reactor with associated limitations on production yield and consistency of the resulting integrated circuits or other semiconductor items being produced.

More complex control schemes have been devised, but these more complex schemes frequently are so complex computationally that on-line operation is either not possible or not feasible. More complex control schemes have also in some cases not been used because of difficulties in achieving required control system tuning and maintenance at the production facility. This has been of somewhat greater concern with regard to controllers

operated by engineers who do not have strong control system backgrounds. As a result is it often difficult for them to resolve all of the complexities imposed in adjusting the control system to the variations in their specific processor performance. This is exacerbated by variations in the same processor with time and changing conditions.

The temperature control problems encountered in thermal processing of semiconductor devices can be thought of in several different ways. One control problem involves matching the wafer temperature to the desired overall or average target or recipe temperature of the processor. The problem involves both achieving the desired recipe temperature and in achieving relatively consistent temperatures from one production run to another.

The desired overall or average recipe temperature of the processor can conveniently be thought of in terms of three different phases. The first phase is typically a ramp-up phase wherein the average operating temperature increases or ramps from a low level when processing is begun. The temperature ramp-up phase is thereafter typically followed by a period during which a desired maximum or other constant processing temperature is maintained. Such a constant temperature phase includes a stabilization period during which the changing temperature ramp ends and a constant or near constant temperature is achieved. Constant temperature phases may occur one or more times in a processing cycle. A further phase is the ramp-down phase wherein the average temperature of the

processor in decreasing. Appreciate that various processes may include more than one of each of these three different phases.

Whether simple or more complex temperature plans or recipes are used, each phase may further be complicated by the introduction of one or more supplementary processing gases or vapor phase processing constituents which affect temperature and thermal response. Such supplementary processing gases are typically gases containing dopants, deposition materials or steam.

Another temperature control problem is to achieve relatively similar temperature exposures or histories during a processing cycle for each of the wafers or other semiconductor workpieces being processed within a batch. Temperature variations routinely occur with regard to wafers positioned near the ends of the array of wafers held within a processing furnace. There may also be other less predictable variations from wafer to wafer, such as along the array of wafers contained within the processing array.

A still further temperature control problem is associated with temperature variations across an individual wafer or other semiconductor workpiece being processed. This area of variability is exemplified by the geometry of most processing furnaces which have a grouping of multiple electrical heating elements formed in rings which surround the array of wafers being processed. Heat from the heating elements is being radiated through the processing vessel and variations can occur with regard to the heat gain experienced by the peripheral

areas of the wafer as compared to the interior areas. Variations in the degree of radiant heat transfer and radiant shadowing which occur from wafer to wafer further exacerbates this problem.

Another noteworthy consideration is the manufacturing concern to minimize the processing time used to effect a particular process or group of processes being carried out with the thermal processor. Minimizing the processing time will typically increase the ramp-up phase temperature change rate. Conversely, time concerns will also increase the ramp-down phase temperature change rate. Increased rates of temperature change cause greater difficulties in maintaining recipe temperatures during the processes of transitioning between ramp-up and stabilization phases, and between stable temperatures and relatively rapid temperature ramp-down phases.

Given these complexities and somewhat countervailing considerations, there is great difficulty in achieving improved control systems which are both practical and workable for improved thermal processing of semiconductor wafers.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1A is a side elevational view, partially in section, of a thermal reactor system embodying the invention.

Fig. 1B is a side elevational view, partially in section, of the thermal reactor system of Fig. 1A during modeling and characterization using thermocouple instrumented wafers.

Fig. 2 is a block diagram illustrating a preferred temperature controller according to the invention.

Fig. 3 is a block diagram illustrating operation of a process sequencing subsystem and gas interface.

Fig. 4 is a block diagram illustrating operation of a temperature subsystem.

Fig. 5 is a waveform diagram illustrating an exemplary pseudo-random binary sequence used to characterize the reactor of Fig. 1A.

Fig. 6 is a control diagram of a characterization control mode which uses the pseudo-random binary sequence of Fig. 2 to characterize the reactor of Fig. 1A prior to actual use in processing semiconductor wafers.

Fig. 7 is a control diagram of an element control mode logic circuit, which employs a spike controller.

Fig. 8 is a control diagram of a base control mode logic circuit, which employs a profile controller and the spike controller of Fig. 7.

Fig. 9 is a control diagram of a dynamic control mode logic circuit, which employs a wafer controller, the profile

controller of Fig. 8, and the spike controller of Fig. 7.

Fig. 10 is a control diagram of a Dt control mode logic circuit, which employs a Dt non-linear controller, the profile controller of Fig. 8, and the spike controller of Fig. 7.

Fig. 11 is a flowchart illustrating design of the preferred controllers.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

The invention provides controllers and methods for controlling a thermal reactor or processor used to process semiconductor workpieces. The typical thermal reactor includes a heating element powered by a power source, and has profile thermocouples and spike thermocouples. A preferred method comprising the following steps: modeling thermal dynamic characteristics of the thermal reactor, the modeling step including providing thermocouple instrumented wafers in the thermal reactor, perturbing the thermal reactor by controlling the heating element using a stimulation sequence, and developing models based on changes in temperature created by the perturbations, the models including a model of power versus spike thermocouple readings, a model of spike thermocouple readings versus profile thermocouple readings, and a model of profile and spike thermocouple readings versus thermocouple instrumented wafer readings.

One aspect of the invention provides a controller unit for controlling a thermal reactor supporting a heating element powered by a power source, profile thermocouples and spike thermocouples, and selectively receiving thermocouple instrumented wafers, the controller unit comprising an input

device receiving a recipe; and a plurality of selectable control mode logic circuits communicating with the profile thermocouples and spike thermocouples, the control mode logic circuits being used to control the heating element relative to the recipe.

Another aspect of the invention provides a method for controlling a thermal reactor including a thermal reactor supporting a heating element powered by a power source, profile thermocouples, and spike thermocouples, and selectively receiving thermocouple instrumented wafers, the method comprising the following steps: modeling thermal dynamic characteristics of the thermal reactor using the profile thermocouples, spike thermocouples, and instrumented wafers; receiving a recipe including desired temperatures with respect to time, and the recipe including desired control modes with respect to time; and switching from one control mode to another in accordance with the recipe, and controlling temperature differently in the different control modes, using temperature information obtained from the profile thermocouples and spike thermocouples.

Another aspect of the invention provides a controller unit for controlling a thermal reactor supporting a heating element powered by a power source, profile thermocouples and spike thermocouples, the controller unit comprising: an on-line model which predicts wafer temperature; and a plurality of selectable control mode logic circuits which control the heating element in response to the on-line model, and

temperature information obtained from the profile thermocouples, and spike thermocouples during operation.

Another aspect of the invention provides a method of controlling a thermal reactor supporting a heating element powered by a power source, profile thermocouples, and spike thermocouples, the method comprising: controlling energy provided to the thermal reactor relative to desired energy, by using measurements from profile thermocouples and taking the integral of $e^{(-2/kT)}$ where k is Boltzmann's constant and T is temperature measured using the profile thermocouples.

Another aspect of the invention provides a controller unit for controlling a thermal reactor supporting a heating element powered by a power source, profile thermocouples and spike thermocouples, the controller unit comprising: a thermal budget controller which controls energy provided to the thermal reactor relative to desired energy, by using measurements from profile thermocouples and taking the integral of $e^{(-2/kT)}$ where k is Boltzmann's constant and T is temperature measured using the profile thermocouples.

Another aspect of the invention provides a method for controlling a thermal reactor including a thermal reactor supporting a heating element powered by a power source, profile thermocouples and spike thermocouples, the method comprising the following steps: modeling thermal dynamic characteristics of the thermal reactor; receiving a recipe including desired temperatures with respect to time, and the recipe including desired control modes with respect to time; and switching from

one control mode to another in accordance with the recipe, and controlling temperature differently in the different control modes, using temperature information provided by the profile thermocouples and spike thermocouples, the control modes being defined by cascaded controllers.

Another aspect of the invention provides a controller unit for controlling a thermal reactor supporting a heating element powered by a power source, profile thermocouples and spike thermocouples, the controller unit comprising: an on-line model which predicts wafer temperature; and a plurality of cascaded selectable control mode logic circuits which control the heating element in response to one or more of: the profile thermocouples, spike thermocouples, and the on-line model.

Another aspect of the invention provides a controller unit for controlling a thermal reactor supporting a heating element powered by a power source, profile thermocouples and spike thermocouples, the controller unit comprising an on-line model which predicts wafer temperature based on measurements from the spike and profile thermocouples; and a plurality of selectable control mode logic circuits, the control mode logic circuits including a base control mode logic circuit having a spike controller which controls power supplied to the heating element in response to measurements by the spike thermocouples, and a profile controller which controls the spike controller in response to measurements by the profile thermocouples; a thermal budget control mode logic circuit which measures energy provided to the thermal reactor and controls energy provided to

the thermal reactor with respect to desired energy, the thermal budget control mode logic circuit employing the spike controller, and the profile controller, and the thermal budget control mode logic circuit further including a Dt controller controlling the profile controller; and a dynamic control mode logic circuit which controls energy provided to the thermal reactor based on predicted wafer temperature, the dynamic control mode logic circuit employing the spike controller, the profile controller, and the on-line model, the dynamic control mode logic circuit further including a wafer controller in communication with the on-line model and controlling the profile controller.

Fig. 1A shows a thermal reactor system 10 embodying the invention. The thermal reactor system 10 includes a thermal reactor 12. The thermal reactor 12 can either be horizontal or vertical in orientation.

The thermal reactor 12 includes a process tube 14 defining a chamber. The process tube 14 is preferably made of quartz, or silicon carbide. In the illustrated embodiment, the process tube is in the general shape of a hollow cylinder having an open end 16. The process tube 14 has a length which extends along and substantially defines a longitudinal axis. The thermal reactor system 10 further includes a boat loader or paddle 18 which inserts or removes a wafer load 20 into or from the process tube 14. More particularly, the boat loader 18 includes a support portion 22, and a door portion 24 which is movable with the support portion and which closes the open end

of the process tube 14 when the support portion 22 is inserted into the process tube. The door portion 24 seals and insulates the process tube to prevent heat loss after the wafer load 20 has been inserted into the process tube 14.

The wafer load 20 includes a plurality of boats 26. In the illustrated embodiment, the boats 24 are formed of quartz or silicon carbide. The wafer load 20 further includes a plurality of silicon wafers 26, and each boat 24 supports a plurality of the wafers 26. In the illustrated embodiment, wafers on each boat 24 are equally spaced. The boat or boats of wafers 26 generally form a wafer or other semiconductor workpiece processing array.

The thermal reactor 12 includes a heating element 30 surrounding the process tube 14. In the illustrated embodiment, the heating element 30 is an electrical resistance heating coil or coils extending along the length of the processing chamber parallel to the length of the process tube 14. The heating element 30 is subdivided into a plurality of separately controllable heating zones 32. The zones 32 are defined by providing connections along the coil to divide the coil or coils into the separately controllable zones. The zones are then separately controllable by supplying power to opposite ends of each zone associated coil or portion of a larger coil. More particularly, the thermal reactor system 10 further includes (Fig. 4) high current voltage transformers 33 and silicon controlled rectifiers (SCRs) 34 for controllably applying power to each of the heating zones 32.

The thermal reactor 12 further includes ceramic insulation 35 encasing the heating element 30. The insulation also serves to reflect and otherwise direct heat toward the wafer array and serves to provide a more uniform layer to minimize heat flux variations away from the processing array.

The thermal reactor 12 further includes a plurality of spike thermocouples 36. Thermocouples as the term is used herein encompasses potentially a variety of temperature sensors, including the more specific meaning of thermocouples. Alternative temperature sensor constructions are intended by the use of the term thermocouples. The spike thermocouples 36 are placed at a suitable location, such as between the heating element 30 and the process tube 14. The spike thermocouples 36 are spaced apart along the length of the of the heating element 30, and a spike thermocouple 36 is located in each of the heating zones 32. The spike thermocouples 36 provide the most specific and responsive indications of the temperature at or of the heating elements in each of the heating zones.

The thermal reactor 12 further includes a profile temperature sensor sheath 38 extending inside the process tube 14. The process tube 14 has a bottom surface, and the process tube 14 is supported on the bottom surface of the process tube 14 in an orientation parallel to the length of the process tube. The sheath 38 extends at least partially across each of the heating zones 32. In the illustrated embodiment, the sheath 38 is formed of quartz or silicon carbide.

The thermal reactor 12 further includes an elongated

profile rod 40 supported in the sheath 38. The profile rod 40 has a length parallel to the length of the process tube 14. The profile rod 40 includes a plurality of thermocouples 42 equally spaced apart along the length of the rod 40, and one thermocouple 42 is located in each of the heating zones 32. The thermocouples 42 are not necessarily aligned with the spike thermocouples 36 in the direction of the length of the process tube 14. The profile rod 40 measures temperature inside the process tube 14 and provides an indication of the temperature of the wafer load 20 in each of the heating zones.

A plurality of thermocouple instrumented wafers 44 are optionally employed during modeling of the thermal reactor. Fig. 1B shows the thermal reactor 12 of Fig. 1A receiving the thermocouple instrumented wafers 44 during modeling. These thermocouple instrumented wafers 44 are uniformly spaced across the wafer load 16 to provide an accurate measurement of the actual temperature of the wafers 28. The wafers or other workpieces being formed of silicon or other semiconductor materials being processed. Each of the exemplary thermocouple instrumented wafers 44 includes a silicon wafer, and two thermocouples 46 bonded to the silicon wafer: one on the edge of the wafer, and one on the center of the wafer. The thermocouples 46 of each thermocouple instrumented wafer 44 are bonded to the silicon wafer, such as with a ceramic adhesive, to provide accurate temperature measurements.

The thermal reactor system 10 further includes a gas delivery system or gas panel 48 controllably injecting process

gases from selectable gas supplies 50 into the process tube 14 to grow, diffuse, or deposit material on the surface of the silicon wafers 28. The gas panel 48 includes (Fig. 3) valves 52 and mass flow controllers 54. The mass flow controllers 52 are used to measure and control flows of process gasses into the process tube 14.

In some embodiments, the process tube 14 is pressurized for low pressure chemical vapor deposition (LPCVD) processes. In these embodiments, the thermal reactor 12 further includes (Fig. 3) a pressure controller 56. In these embodiments, the thermal reactor system 10 further includes a baratron or other suitable pressure sensing device 58 which measures the pressure in the process tube and communicates the measured pressure to the pressure controller 56. Further, in these embodiments, the thermal reactor system 10 further includes pumps and valves 60, in communication with the pressure controller 56, to achieve the desired pressure in the process tube 14.

In some embodiments, the thermal reactor 12 further includes (Fig. 3) a torch 62 internal or external to the process tube 14. The torch 62 is used for wet oxidation processes by burning a ratio of hydrogen and oxygen to produce steam in the process tube 14.

The thermal reactor system 10 includes (Fig. 2) a control system 64 controlling the thermal reactor 12. The control system 64 includes two subsystems: a process sequencing subsystem 66 for process sequencing, and a temperature subsystem 68 for temperature control. Each subsystem 64 and 66

includes a microprocessor, such as an Intel PC, 286, 386, 486, Pentium, or higher, or clone thereof, or Motorola 6800, 68000 or higher, or other microprocessor.

While other microprocessors can be used, in the illustrated embodiment, the process sequencing subsystem 66 employs a 6800 microprocessor 70. The process sequencing subsystem includes random access memory 72 and a programmable EPROM 74 that stores controller logic. The process sequencing subsystem 66 further includes a plurality of digital input and output channels 76 as well as a plurality of analog input and output channels 78. The process sequencing subsystem 66 further includes a plurality of serial input and output channels 80 for external (remote) communication, if external communication is desired. The process sequencing subsystem 66 follows a user defined process recipe. More particularly, the thermal reactor system 10 further includes a user interface 82 defining an input device. While other user interfaces can be employed, in the illustrated embodiment the user interface 82 comprises a touch screen terminal interface with which a user can enter a user defined process recipe. In the process recipe, the user can define, on a per step basis, step time, gas flows, chamber pressure, temperature setpoints, and ramp rates.

While other microprocessors can be employed, in the illustrated embodiment, the temperature subsystem 68 includes a 486 microprocessor 84. The temperature subsystem 68 further includes dynamic random access memory 86 for use with the

microprocessor 84. For example, in the illustrated embodiment, the temperature subsystem 68 controller unit includes four megabytes of dynamic random access memory. The temperature subsystem 68 controller unit of the illustrated embodiment further includes a two megabyte flash disk 88, a dual ported random access memory 90, a sixteen bit analog to digital converter 92, and a PC/104 bus 94. The temperature subsystem includes a plurality of multivariable controllers 96, 98, 100, and 102 constructed using robust optimal control theory with empirically derived models of the furnace and wafers. More particularly, in the illustrated embodiment, the multivariable controllers 96, 98, 100, and 102 are constructed using H-Infinity control theory.

In the illustrated embodiment, the control system 64 further includes (Fig. 3) a gas panel interface 104 connected between the gas panel 48 and the process sequencing subsystem 68. The gas panel interface 104 provides the control system 64 with an interface to communicate with the mass flow controllers 54, the gas valves 52, the internal or external torch 62, the pressure controller 56, the boat loader 18, etc. Further, the gas panel interface 104 includes a plurality of hardware safety interlocks for the thermal reactor (e.g., to ensure hydrogen flow with a proper oxygen to hydrogen ratio, to detect a flame from the torch 62, etc.).

In the illustrated embodiment, the control system 64 further includes (Fig. 4) a temperature interface connected between the thermocouples 36, 42, and 44 and the temperature

subsystem 68. More particularly, in the illustrated embodiment, the temperature interface comprises thermocouple amplifier interface boards 106. In the illustrated embodiment, the temperature subsystem communicates with up to two thermocouple amplifier interfaces: one for measuring spike and profile thermocouples 36 and 42, and one for measuring the thermocouples 46 of the thermocouple instrumented wafers 44 (if thermocouple instrumented wafers are employed). In the illustrated embodiment, the control system 64 further includes (Fig. 4) an element firing interface 108 connected between the heating element 30 and the temperature subsystem 68. The element firing interface 108 includes one firing board for each of the defined heating zones 32. These firing boards use a zero-point switching technique to apply or discontinue power at zero crossings of the voltage waveform.

A process of designing the controllers 96, 98, 100, and 102 is illustrated in detail in Fig. 11.

In a characterization control mode (Fig. 6, and step 110 of Fig. 11), the thermal dynamic characteristics of the thermal reactor are modeled using spike, profile, and wafer temperatures as well as power setpoints during excitation using a random or other stimulation sequence (Fig. 5). In the illustrated embodiment, a pseudo-random binary sequence (PRBS) is employed. More particularly, in the characterization control mode (Fig. 6), the thermal reactor is brought up to operating temperature and then perturbed using the pseudo-random binary sequence, causing gradual temperature

fluctuations in the thermal reactor. In steps 112a-d, models are created based on changes in temperature created by the perturbations. In the illustrated embodiment, all models are derived using a linear least squares minimum distance system identification technique. In the illustrated embodiment, all models are represented and implemented in state-space form.

In the illustrated embodiment, two types of models are created: off-line and on-line. By "off-line model," what is meant is a model that is created for control system design. By "on-line model," what is meant is a model that is active during the operation of the thermal reactor 12, such as to process actual semiconductor wafers 28.

In the illustrated embodiment, three off-line models are developed: a power setpoint vs. spike thermocouple model; a spike thermocouple vs. profile thermocouple model; and a profile and spike thermocouple vs. thermocouple instrumented wafer model. Each off-line model is used to design the controllers 96, 98, 100, and 102 in the temperature subsystem.

In the illustrated embodiment, a single on-line model 114 is developed to estimate wafer temperature during operation of the thermal reactor 12. The on-line model 110 predicts the actual temperature of the wafers 28 using real temperature measurements from the spike and profile thermocouples 36 and 42. Because modeling of the entire thermal reactor 12 is complicated and very susceptible to variations and maintenance operations over time, simple modeling of the relationship between the wafer temperatures and the measured profile and

spike temperatures is performed to provide an accurate indication of the wafer temperatures during dynamic changes in temperature. Further, it is assumed that under steady-state conditions the profile temperatures are indicative of the actual temperatures of the wafers 28.

After modeling, in steps 116a, 116b, and 116c (Fig. 11), the three off-line models are used to create three separate and unique controllers: the spike controller 96, the profile controller 98, and the wafer controller 100. The spike controller 96 uses the difference between the spike setpoints and spike thermocouple measurements as inputs, and then outputs the power setpoints to the firing interface 108. The profile controller 98 uses the difference between the profile setpoints and the profile measurements as inputs and then outputs spike setpoints to the spike controller 96. The wafer controller 100 uses the difference between the wafer setpoints and predictions of the on-line wafer temperature model as inputs and then outputs profile setpoints to the profile controller 98. In the illustrated embodiment, each controller 96, 98, and 100 is designed using H-Infinity robust optimal control theory. More particularly, in the illustrated embodiment, each of these controllers are multivariable, in which the interaction between heating zones is taken into consideration to provide improved temperature response to the desired ramp or setpoint.

The design of the controllers 96, 98, and 100 will now be described in greater detail. The controllers 96, 98, and 100 are designed using data obtained from an identification

experiment. The design procedure comprises two main steps; namely, system identification and controller design. The preferred embodiment employs high performance numerical analysis software such as MATLAB (TM) and SIMULINK (TM) in modeling and in controller design.

System Identification or Characterization

The system identification or characterization step involves making empirical measurements of the processor temperature response characteristics in response to known thermal input. The response is measured by the spike thermocouples 36, profile thermocouples 42 and the temperature sensing wafers 46. The measured response data is analyzed using a suitable analytical technique to achieve a model or models which provide predictive indication of wafer temperatures based upon the spike and profile thermocouple temperatures which can be measured during actual processing of wafers. However, to achieve the needed system thermal response characterization it is necessary to utilize the temperature sensing wafers 46 or other measuring techniques which at least at this time must be done in a separate characterizing phase before actual operational processing begins.

One preferred technique for deriving the characterization information involves using a least-squares parameter estimation algorithm to obtain estimates of the system parameters which reflect temperature response characteristics. The main objectives of this step are the identification of a system

model that describes the input-output data and the estimation of uncertainty bounds that describe the confidence in the model. For this purpose, we consider systems described by the general state-space model:

$$=Ax+Bu; \quad y=Cx+Du$$

where x is the state vector, u is the input vector having m number of inputs, and y is the output vector having n number of outputs. Matrix A has dimensions n x n. Matrix B has dimensions n x m. Matrix C has dimensions m x n. And matrix D has dimensions m x m. The coefficients of the matrices are parameters which are derived and potentially adjusted for the particular model being developed to optimize the model's successful operation.

Assuming that (A,C) is observable (all modes of the state-space equation can be observed at the output), the above model can be written as:

$$=(A-LC)x+(B-LD)u+Ly; \quad y=Cx+Du$$

where A-LC is a Hurwitz matrix (see various texts on control theory, such as Kailath, T., *Linear Systems*, Prentice-Hall, Englewood Cliffs, NJ, 1980).

This implies that the above linear system can be described by:

$$=Fx+\Theta_1 u+\Theta_2 y; \quad y=qx+du$$

where (F,q) is observable, F is the Hurwitz matrix and Θ_1, Θ_2, and d are matrices representing the adjustable parameters of the model.

By taking a Laplace transform of the previous equation, we

have:

$$sIx(s)-x(0)=Fx(s)+\Theta_1 u(s)+\Theta_2 y(s);\ \ y(s)=qx(s)+du(s)$$

where I is the identity matrix and x(o) are the initial conditions of the states.

Next, by solving for the states we obtain:

$$x(s)=(sI-Fx)^{-1}[\Theta_1 u(s)+\Theta_2 y(s)+x(0)]$$

Now solving for the output using the above state equation to obtain:

$$y(s)=q(sI-Fx)^{-1}[\Theta_1 u(s)+\Theta_2 y(s)+x(0)]+du(s)$$

Reorganizing into common terms the above equation becomes:

$$y(s)=[q(sI-Fx)^{-1}\Theta_1+d]u(s)+q(sI-F)^{-1}\Theta_2 y(s)+q(sI-F)^{-1}x(0)$$

All are scalar transfer functions, therefore they may be transposed to obtain:

$$y(s)=\Theta_1^T(sI-F^T)^{-1}q^T u(s)+\Theta_{2T}(sI-F^T)^{-1}q^T y(s)+du(s)+x(0)^T(sI-F^T)^{-1}q^T$$

For single-input, single-output systems, the last equation can be written in the convenient for parameter estimation linear model form:

$$y=\Theta^T w$$

where Θ is a vector containing the adjustable parameters Θ_1, Θ_2, d as well as the possibly unknown initial conditions x(0), while w contains the signals $(sI-F^T)^{-1}q^T u$, $(sI-FT)^{-1}q^T y$, u, and $(sI-F^T)^{-1}q^T$.

Thus, the basic system identification step comprises the following sub-steps:

1. Perform an experiment to generate input-output time sequences.

2. Compute the filtered signals w.
3. Estimate the parameters of the linear model $y=\Theta^T w$.
4. Compute the corresponding state-space representation [A,B,C,D] of the identified system.
5. Reduce the order of the identified system, if necessary.
6. Compute error bounds (uncertainty) for the identified system.

These substeps of the system identification step will now be described in greater detail.

The identification or characterization experiment relies on the generation of an input signal which provides sufficient excitation to the thermal reactor so as to allow the reliable identification of its parameters. Several types of excitation signals have been proposed in the literature (see, for example, Ljung, L., *System Identification: Theory for the User*, Prentice-Hall, Englewood Cliffs, NJ, 1980). For reasons of design simplicity, the illustrated embodiment employs the pseudo-random binary sequence (PRBS) to provide the desired excitation. Furthermore, in order to avoid extensive experimentation requirements in selecting the size of the excitation, the identification is performed in closed-loop. That is, prior information about the thermal reactor to be identified is used to design a simple controller (e.g., proportional or proportional-integral). The pseudo-random binary sequence excitation is then fed as a reference input (set-point) to the controller and the resulting control inputs

and thermal reactor outputs are measured.

Although such an approach seems restrictive in that it requires a preliminary controller design, in practice this requirement is not too severe. Typically, elementary crude models of the thermal reactor are available or can easily be derived or, as it is often the case, simple controllers have been already implemented. Practical experience indicates that the identification results are not too sensitive to the controller used as long as its bandwidth and performance are reasonable. Of course, if this is not the case, the identification and controller design steps can be iterated using the new controller in the next identification experiment, until adequate performance is obtained.

The design of the pseudo-random binary sequence requires more attention. This type of excitation is implemented as a sequence of step changes in the reference commands about the nominal operating condition of the thermal reactor. Pseudo-random binary sequences can be defined by two vectors:

$$[t_1, t_2, \Lambda], \ [m_1, m_2, \Lambda]$$

where the first vector indicates switching times and the second indicates the deviation from the nominal set-point (± maximum deviation level). The randomness in the pseudo-random binary sequence enters in the switching times where $t_{i+1}-t_i$ is a random number. The maximum level and the minimum and maximum duration of each pulse are the design parameters of a pseudo-random binary sequence. In general, the level should be selected as large enough to provide a good signal-to-noise ratio (SNR) but

small enough so as to avoid big deviations from the nominal operating condition, which will introduce interference from the ever-present plant nonlinearities. This is precisely where closed-loop identification has an advantage because even a crude controller will keep the plant response around the nominal within, roughly, the PRBS level. The duration of each pseudo-random binary sequence pulse should be such that the resulting sequence has most of its power around the desired closed-loop bandwidth (and closed-loop crossover) which is where the reactor model should be reliable. Finally, the total length of the pseudo-random binary sequence is dictated by memory and experiment-time limitations, but it should be long enough to allow for noise averaging and the observation of the plant response at a sufficient number of frequencies. Roughly, a rule of thumb is to observe the response of the thermal reactor to 7-10 PRBS pulses whose duration is selected according to the previous criteria.

For multivariable system identification, multiple PRBS inputs must be generated, one for each channel. These should be further restricted to be independent of each other, in the sense that the resulting regressor vector has a well-conditioned covariance matrix. This requirement does not present a problem when long sequences are used. In practice, however, the limited length of the sequence suggests that the validity of this assumption should be checked and the PRBS regenerated if the condition fails.

As previously mentioned, a standard least squares

algorithm is used to estimate the parameters of the linear model which are then used to compute the entries of the state-space matrices according to the equations presented above. In addition to this, the parameter estimation algorithm is modified in order to improve its reliability and its ability to yield estimates that emphasize the fit of the plant characteristics in a given frequency range (weighted least-squares). The latter is achieved in a straightforward manner by filtering the input-output data numerically, with a filter that has a desired frequency response. For example, a low-pass filter could be used in cases of data corrupted by high-frequency noise, while a band-pass filter could be used to enhance the reliability of the identified model around the desired closed-loop bandwidth. The success of the identification and the possible redesign of these filters are judged based on "uncertainty" bounds that are discussed subsequently. It should be emphasized that although some iterations may be required in the parameter estimation step, these do not necessarily require repetition of the identification experiment.

Further, and in order to improve the numerical reliability of the estimator, singular value decomposition methods are employed to compute the least-squares solution. In addition to this, the estimation step solves, in one embodiment, the following problem

$$\text{Min } \|H\Theta\|, \text{ subject to: } \|y - \Theta w\| \leq (1+\rho)\, E_{LS}$$

where H is a weighting matrix, ρ is a threshold parameter and

E_{LS} is the error corresponding to the least-squares solution. While this problem can be solved easily in closed form, its solution possesses some interesting properties. That is, by choosing the threshold parameter to be sufficiently "small" (e.g., 0.5) the quality of the estimated parameters measured by the estimation error deteriorates in a controlled fashion, by at most a factor of $(1+\rho)$. This allows the flexibility to adjust the estimated parameters so as to reflect more subtle estimation objectives. For example, by appropriately choosing the weighting matrix H, the solution of the above minimization can emphasize coupling and/or stability properties of the identified model. This ability has been found to be beneficial in cases of noisy data where the noise may cause the reactor to appear as more coupled than it is in "reality." Alternatively, it may be desirable for a reactor model to be as decoupled as possible, something that simplifies the controller design and can possibly improve its robustness to reactor variations.

The obtained reactor model is then checked for minimality using standard reduction algorithms, (see Chiang, R. and M. Safonov, *Robust Control Toolbox: User's Manual (For use with MATLAB)*, The Mathworks Inc., Natick, MA, 1992) and references therein, and the reliability of the model is quantified by analysis of residuals. This step quantifies confidence in the model and provides constraints that should be met during the controller design step. In particular, performing a spectral analysis on the estimation error provides estimates of the effective multiplicative and feedback uncertainty (see

Alexander, C. and K.S. Tsakalis, "Control of an Inverted Pendulum: A Classical Experiment Revisited," *Proc. 1995 Western Multiconference, Society for Computer Simulation*, Las Vegas, 1995). These estimates represent bounds that the closed-loop sensitivity and complementary sensitivity should satisfy so that the designed controller will stabilize the actual reactor. It should be pointed out that the computations provide only an estimate of these bounds. In a strict sense, closed-loop stability cannot be guaranteed. However, there appears to be a very strong correlation between these bounds and successful controller designs.

Controller Design

The core of the controller design procedure is the H^∞ design approach (see Chiang, R. and M. Safonov, *Robust Control Toolbox: User's Manual (For use with MATLAB)*, The Mathworks Inc., Natick, MA, 1992), augmented by controller reduction and well-posedness checks. More specifically, the uncertainty bounds resulting from the system identification step are used to define sensitivity and complementary sensitivity weights. These, together with the identified reactor, augmented by integrators, form the so-called super-plant in the format required by standard H^∞ computational software. Typically, the resulting H^∞ controller is of high order and contains states due to the weights that are essentially irrelevant for its performance and can potentially degrade its reliability, robustness and discretization properties. For this reason, the reduction is performed in three steps.

The first step is to remove states that correspond to very fast modes, e.g., two orders of magnitude above the closed-loop bandwidth. Typically, such modes are irrelevant to the controller stability or performance but they create problems in digital implementation since their discrete-time approximation requires high sampling rates. The next step is to remove very slow modes which again contribute very little to the overall closed-loop behavior. Such modes are typically associated with "pole-zero cancellations" near the jw-axis and, if retained, may cause the appearance of small but slowly decaying errors in the tracking performance. Finally, a standard model order

reduction (weighted or not) is performed to eliminate other controller states that have insignificant contribution. The reduction step is a price paid in order to simplify the weight selection step. Even though a verification is made that the reductions did not cause any significant performance deterioration, this verification is relatively straightforward and can be performed easily with standard computational tools, e.g., (see Chiang, R. and M. Safonov, *Robust Control Toolbox: User's Manual (For use with MATLAB)*, The Mathworks Inc., Natick, MA, 1992, and Zhou, K., J. Doyle and K. Glover, *Robust and Optimal Control*, Prentice-Hall, Englewood Cliffs, NJ, 1996).

The above procedure computes a controller of reasonable order that exhibits good performance with the linearized model of the reactor. That is, the actual system is expected to exhibit similar performance locally around the operating point. For a successful controller implementation, however, saturation nonlinearities that are invariably present in all actuators, e.g., heating elements, should be considered. The main problem caused by such saturations is the so-called integrator wind-up. Typical anti-windup modifications include the use of a stabilizing feedback around the compensator that is activated by a dead-zone type nonlinearity when the controller output (control input) exceeds the saturation level (see Astrom, K.J. and B. Hagglund, *PID Controllers: Theory, Design and Tuning*, ISA Research Triangle Park, NC, 1994).

A simple way to achieve this in the multivariable case, is

by feeding back to the compensator an auxiliary signal "v" computed as

$$v = Lud(u)$$

where u is the control input, d(u) is a scalar, dead-zone-like signal quantifying the level of saturation (d(u)=0 when the control is not saturated) and L is a matrix gain such that the closed-loop system of the controller and L is stable. An effective design of L can be obtained as an observer gain (see Anderson, B.D.O. and J.B. Moore, *Optimal Control: Linear Quadratic Methods*, Prentice-Hall, Englewood Cliffs, NJ, 1990). In this case, the controller-observer gain system can be nicely interpreted as the construction of an observer which forces the controller output to track the output of a system that consists of the controller composed with the saturation nonlinearity. This, together with the minimality of the controller ensure that its states, and in particular those associated with the integrators cannot grow unbounded. Furthermore, in the design of the observer gain, the directionality properties of the controller can be preserved as much as possible, so that the controller saturation does not completely destroy the output decoupling achieved by the linear design.

Finally, as a last step in the controller design procedure, an evaluation step is performed via nonlinear simulation of the discretized controller and identified reactor, together with the actuator saturation. This evaluation has been very useful in exposing possible design

limitations and assessing the controller capabilities, e.g., in terms of achievable ramp rates. Practical experience indicates that the simulated behavior of the closed loop system is indeed a good approximation of the actual one.

After design, in step 118, the spike, profile, and wafer controllers 96, 98, and 100 and the on-line wafer model are implemented in hardware in the temperature subsystem 68.

In the illustrated embodiment, a control mode logic circuit is selectable from among different available control mode logic circuits including an element control mode logic circuit (Fig. 7) defining an element control mode, a base control mode logic circuit (Fig. 8) defining a base control mode, a dynamic control mode logic circuit (Fig. 9) defining a dynamic control mode, and a Dt control mode logic circuit (Fig. 10) defining a Dt control mode. Each of these control mode logic circuits are defined by a single one or a combination of the controllers 96, 98, and 100.

More particularly, the temperature subsystem 68 employs the spike controller 96 for the element control mode (Fig. 7). The temperature subsystem 68 employs the spike controller 96 injected with the pseudo-random binary sequence for the characterization control mode (Fig. 6). The temperature subsystem 68 employs a combination of the profile controller 98 and the spike controller 96 for the base control mode (Fig. 8). The temperature subsystem 68 employs a combination of the wafer controller 100, the profile controller 98, and the spike controller 96 for the dynamic control mode (Fig. 9). The

temperature subsystem 68 employs the non-linear Dt controller 102 with the profile controller 98, and the spike controller 96 to provide the Dt control mode (Fig. 10).

A user can provide a recipe comprising multiple steps and which uses any one of the control modes in each step. For example, a user can provide a recipe that switches from one control mode to another at a given stage of semiconductor processing. One suggested approach is to employ the base control mode during a furnace check and push in of the boat 18, prior to a ramp up in temperature, to employ the wafer control mode during temperature ramp up and temperature stabilization, to employ the Dt control mode during wafer processing steps, and to employ the base control mode during boat push out. Another suggested approach is to use the base control mode during all processing steps.

The element control mode is typically a maintenance mode (e.g., to burn in elements). In the element control mode, the spike controller controls on the basis of spike thermocouple temperatures. The mode is not used in normal processing of wafers.

The base control mode (Fig. 8) is the default mode of operation. In the base control mode, the profile controller 98 provides a spike setpoint control signal based on a profile error. The profile error is based on the difference between profile temperature setpoint, and profile temperature measurements by the profile thermocouples 42. The spike controller 98 controls power to the thermal reactor based on

spike error. The spike error is based on the difference between spike setpoint and spike temperature measurements by the spike thermocouples 36. The base control mode provides accurate control resulting in improved process uniformity and cycle time reduction attributed to faster stabilization times. The base control mode logic circuit uses the profile and spike controllers simultaneously by cascading them together.

Profile thermocouples do not match temperatures at the edge of a load. Users prefer not to change their recipes to compensate for this. One solution to this problem is to shorten profile thermocouples which results in readings generated by the profile thermocouples more accurately matching temperatures at the edge of a load. The dynamic or wafer control mode (Fig. 9) provides a solution to the problem without requiring modification of the profile thermocouples or adjustment of the user's recipe.

In the dynamic control mode, the wafer controller 100 provides prediction or estimation of the temperatures of wafers 28 and control to achieve temperatures for the wafers 28 which approach the desired or recipe wafer temperatures. The dynamic control mode may be most advantageously employed during temperature ramping and stabilization steps. The dynamic control mode involves the prior use of the thermocouple instrumented wafers 44 during modeling, as discussed above. After modeling, while the control system is in use, the dynamic control mode controls the thermal reactor 12 based on predicted wafer temperature using the on-line wafer temperature

estimating model 114. The on-line wafer temperature estimation model 114 predicts wafer temperature based on measurements from the spike and profile thermocouples 36 and 42. More particularly, wafer temperature is predicted based on measurements from the spike and profile thermocouples 36 and 42 and the relationship between measurements taken by the thermocouple instrumented wafers 44 (representing wafer temperature) and measurements taken by the profile and spike thermocouples 36 and 42 during modeling.

In the dynamic control mode, the wafer controller 100 provides a profile setpoint based on a wafer error. The wafer error is based on the difference between profile temperature setpoint, and profile temperature measurements by the profile thermocouples 42. The profile controller provides a spike setpoint control signal based on profile error. The profile error is based on the difference between profile temperature setpoint produced by the wafer controller 100, and profile temperature measurements by the profile thermocouples. The spike controller controls power to the thermal reactor based on spike error. The spike error is based on the difference between spike setpoint and spike temperature measurements by the spike thermocouples 36. The dynamic control mode uses the spike controller 96, the profile controller 98, and the wafer controller 100 cascaded together.

In the Dt or thermal budget mode, the Dt controller 102 measures temperature exposure or applied thermal energy and controls energy with respect to setpoint or desired energy.

Thermal budget is controlled, using measurements from profile thermocouples 42 and taking the integral of $e^{(-2/kT)}$ where k is Boltzmann's constant and T is temperature measured using the profile thermocouples 42, to maintain Dt values in accordance with desired energy. A calculation is made of energy sent into the thermal reactor, and energy sent into the thermal reactor is controlled. The thermal budget mode is advantageously used to control thermal budget during critical processing steps to maintain consistent Dt values both down the load and run-to-run.

In the Dt control mode (Fig. 10), the Dt controller 102 provides a profile setpoint based on an energy error. The energy error is based on the difference between an energy setpoint, and measured energy. The profile controller 98 provides a spike setpoint control signal based on a profile error. The profile error is based on the difference between profile temperature setpoint produced by the Dt controller, and profile temperature measurements by the profile thermocouples 42. The spike controller 96 controls power to the thermal reactor based on spike error. The spike error is based on the difference between spike setpoint and spike temperature measurement by the spike thermocouples 36.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred

forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.

CLAIMS:

1. A method for controlling a thermal reactor including a heating element powered by a power source, and having profile thermocouples and spike thermocouples, the method comprising the following steps:

modeling thermal dynamic characteristics of the thermal reactor, the modeling step including providing thermocouple instrumented wafers in the thermal reactor, perturbing the thermal reactor by controlling the heating element using a stimulation sequence, and developing models based on changes in temperature created by the perturbations, the models including a model of power versus spike thermocouple readings, a model of spike thermocouple readings versus profile thermocouple readings, and a model of profile and spike thermocouple readings versus thermocouple instrumented wafer readings.

2. A method for controlling a thermal reactor in accordance with claim 0 and further comprising, after the modeling step, selecting a control mode from among a plurality of available control modes.

3. A method for controlling a thermal reactor in accordance with claim 0 wherein one of the available control modes is a thermal budget control mode in which energy provided to the thermal reactor is measured and controlled with respect to desired energy.

4. A method for controlling a thermal reactor in accordance with claim 0 wherein one of the available control modes is a thermal budget control mode wherein energy provided to the thermal reactor is controlled relative to desired energy, by using measurements from profile thermocouples and taking the integral of $e^{(-2/kT)}$ where k is Boltzmann's constant and T is temperature measured using the profile thermocouples.

5. A method for controlling a thermal reactor in accordance with claim 0 wherein one of the available control modes is a dynamic control mode in which power is controllably supplied to the heating element based on predicted wafer temperature, and in which wafer temperature is predicted based on measurements from the spike and profile thermocouples.

6. A method for controlling a thermal reactor in accordance with claim 0 wherein one of the available control modes is a base control mode, in which power is controllably supplied to the heating element in response to profile thermocouple measurements.

7. A controller unit for controlling a thermal reactor including a heating element powered by a power source, and having profile thermocouples and spike thermocouples, and selectively receiving thermocouple instrumented wafers, the controller unit comprising:

an input device receiving a recipe; and

a plurality of selectable control mode logic circuits communicating with the profile thermocouples and spike thermocouples, the control mode logic circuits being used to control the heating element relative to the recipe.

8. A controller unit in accordance with claim 0 wherein the control mode logic circuits comprise H□ controllers.

9. A controller unit in accordance with claim **Error! Reference source not found.** wherein the control mode logic circuits include a thermal budget control mode logic circuit which measures energy provided to the thermal reactor and controls energy provided to the thermal reactor with respect to desired energy.

10. A controller unit in accordance with claim **Error! Reference source not found.** wherein the control mode logic circuits include a thermal budget control mode logic circuit which controls energy provided to the thermal reactor relative to desired energy, by using measurements from profile thermocouples and taking the integral of $e^{(-2/kT)}$ where k is Boltzmann's constant and T is temperature measured using the profile thermocouples.

11. A controller unit in accordance with claim **Error! Reference source not found.** wherein the control mode logic circuits include a dynamic control mode logic circuit which controllably supplies power to the heating element based on predicted wafer temperature, the dynamic control mode logic circuit including an on-line wafer model in which wafer temperature is predicted based on measurements from the spike and profile thermocouples.

12. A controller unit in accordance with claim **Error! Reference source not found.** wherein the control mode logic circuits include a base control mode logic circuit which controls power supplied to the heating element in response to measurements by the profile thermocouples.

13. A method for controlling a thermal reactor including a heating element powered by a power source, and having profile thermocouples, spike thermocouples, and selectively receiving thermocouple instrumented wafers, the method comprising the following steps:

modeling thermal dynamic characteristics of the thermal reactor using the profile thermocouples, spike thermocouples, and instrumented wafers;

receiving a recipe including desired temperatures with respect to time, and the recipe including desired control modes with respect to time; and

switching from one control mode to another in accordance with the recipe, and controlling temperature differently in the different control modes, using the profile thermocouples and spike thermocouples.

14. A method for controlling a thermal reactor in accordance with claim 0 wherein one of the available control modes is a thermal budget mode wherein energy provided to the thermal reactor is measured and controlled with respect to desired energy.

15. A method for controlling a thermal reactor in accordance with claim 0 wherein one of the available control modes is a thermal budget mode wherein energy provided to the thermal reactor is controlled relative to desired energy, by using measurements from profile thermocouples and taking the integral of $e^{(-2/kT)}$ where k is Boltzmann's constant and T is temperature measured using the profile thermocouples.

16. A method for controlling a thermal reactor in accordance with claim 0 wherein one of the available control modes is a dynamic control mode in which power is controllably supplied to the heating element based on predicted wafer temperature, and in which wafer temperature is predicted based on measurements from the spike and profile thermocouples.

17. A method for controlling a thermal reactor in accordance with claim 0 wherein one of the available control modes is a base control mode, wherein a base controller acts in response to profile thermocouple measurements.

18. A controller unit for controlling a thermal reactor including a heating element powered by a power source, and having profile thermocouples and spike thermocouples, the controller unit comprising:

an on-line model which predicts wafer temperature; and

a plurality of selectable control mode logic circuits which control the heating element in response to the on-line model, the profile thermocouples, and spike thermocouples.

19. A controller unit in accordance with claim 0 wherein the control mode logic circuits include a thermal budget control mode logic circuit which measures energy provided to the thermal reactor and controls energy provided to the thermal reactor with respect to desired energy.

20. A controller unit in accordance with claim 0 wherein the control mode logic circuits include a thermal budget control mode logic circuit, which controls energy provided to the thermal reactor relative to desired energy, by using measurements from profile thermocouples and taking the integral of $e^{(-2/kT)}$ where k is Boltzmann's constant and T is temperature measured using the profile thermocouples.

21. A controller unit in accordance with claim 0 wherein the control mode logic circuits include a dynamic control mode logic circuit which controllably supplies power to the heating element based on predicted wafer temperature, the dynamic control mode logic circuit including an on-line wafer model in which wafer temperature is predicted based on measurements from the spike and profile thermocouples.

22. A controller unit in accordance with claim 0 wherein the control mode logic circuits include a base control mode logic circuit which controls power supplied to the heating element in response to measurements by the profile thermocouples.

23. A method of controlling a thermal reactor including a heating element powered by a power source, and having profile thermocouples and spike thermocouples, the method comprising:

controlling energy provided to the thermal reactor relative to desired energy, by using measurements from profile thermocouples and taking the integral of $e^{(-2/kT)}$ where k is Boltzmann's constant and T is temperature measured using the profile thermocouples.

24. A controller unit for controlling a thermal reactor including a heating element powered by a power source, and having profile thermocouples and spike thermocouples, the controller unit comprising:

a thermal budget controller which controls energy provided to the thermal reactor relative to desired energy, by using measurements from profile thermocouples and taking the integral of $e^{(-2/kT)}$ where k is Boltzmann's constant and T is temperature measured using the profile thermocouples.

25. A method for controlling a thermal reactor including a thermal reactor including a heating element powered by a power source, and having profile thermocouples and spike thermocouples, the method comprising the following steps:

modeling thermal dynamic characteristics of the thermal reactor;

receiving a recipe including desired temperatures with respect to time, and the recipe including desired control modes with respect to time; and

switching from one control mode to another in accordance with the recipe, and controlling temperature differently in the different control modes, using the profile thermocouples and spike thermocouples, the control modes being defined by cascaded controllers.

26. A method for controlling a thermal reactor in accordance with claim 0 wherein the temperature in the thermal reactor is selectively ramped up to operating temperature, and wherein the control modes provide full time cascade control, including cascade control after the temperature is ramped up.

27. A method for controlling a thermal reactor in accordance with claim 0 wherein one of the available control modes is a base control mode in which a spike controller acts in response to spike thermocouple measurements, and in which a profile controller acts in response to profile thermocouple measurements and controls the spike controller.

28. A method for controlling a thermal reactor in accordance with claim 0 wherein one of the available control modes is a thermal budget mode in which a spike controller acts in response to spike thermocouple measurements, in which a profile controller acts in response to profile thermocouple measurements and controls the spike controller, and in which a Dt controller measures energy provided to the thermal reactor and controls energy provided to the thermal reactor with respect to desired energy and controls the profile controller.

29. A method for controlling a thermal reactor in accordance with claim 0 wherein one of the available control modes is a thermal budget mode in which a spike controller acts in response to spike thermocouple measurements, in which a profile controller acts in response to profile thermocouple measurements and controls the spike controller, and in which a Dt controller controls energy provided to the thermal reactor relative to desired energy, by using measurements from profile thermocouples and taking the integral of $e^{(-2/kT)}$ where k is Boltzmann's constant and T is temperature measured using the profile thermocouples, the Dt controller controlling the profile controller.

30. A method for controlling a thermal reactor in accordance with claim 0 wherein one of the available control modes is a dynamic control mode in which a spike controller acts in response to spike thermocouple measurements, in which a profile controller acts in response to profile thermocouple measurements and controls the spike controller, an in which a wafer controller acts in response to predicted wafer temperature using an on-line wafer temperature estimation model to predict the wafer temperature, the wafer controller controlling the profile controller.

31. A controller unit for controlling a thermal reactor supporting a heating element powered by a power source, profile thermocouples and spike thermocouples, the controller unit comprising:

an on-line model which predicts wafer temperature; and

a plurality of cascaded selectable control mode logic circuits which control the heating element in response to one or more of: the profile thermocouples, spike thermocouples, and the on-line model.

32. A controller unit in accordance with claim 0 wherein the control mode logic circuits include a base control mode logic circuit including a spike controller which controls power supplied to the heating element in response to measurements by the spike thermocouples, and a profile controller which controls the spike controller in response to measurements by the profile thermocouples.

33. A controller unit in accordance with claim 0 wherein the control mode logic circuits include a thermal budget control mode logic circuit which measures energy provided to the thermal reactor and controls energy provided to the thermal reactor with respect to desired energy, the thermal budget control mode logic circuit including a spike controller which controls power supplied to the heating element in response to measurements by the spike thermocouples, a profile controller which controls the spike controller in response to measurements by the profile thermocouples, and a Dt controller controlling the profile controller.

34. A controller unit in accordance with claim 0 wherein the control mode logic circuits include a thermal budget control mode logic circuit which measures energy provided to the thermal reactor and controls energy provided to the thermal reactor with respect to desired energy, the thermal budget control mode logic circuit including a spike controller which controls power supplied to the heating element in response to measurements by the spike thermocouples, a profile controller which controls the spike controller in response to measurements by the profile thermocouples, and a non-linear controller controlling the profile controller.

35. A controller unit in accordance with claim 0 wherein the control mode logic circuits include a thermal budget control mode logic circuit which measures energy provided to the thermal reactor and controls energy provided to the thermal reactor with respect to desired energy, by using measurements from the profile thermocouples and taking the integral of $e^{(-2/kT)}$ where k is Boltzmann's constant and T is temperature measured using the profile thermocouples, the thermal budget control mode logic circuit including a spike controller which controls power supplied to the heating element in response to measurements by the spike thermocouples, a profile controller which controls the spike controller in response to measurements by the profile thermocouples, and a Dt controller controlling the profile controller.

36. A controller unit in accordance with claim 0 wherein the control mode logic circuits include a dynamic control mode logic circuit which controllably supplies power to the heating element based on predicted wafer temperature, and includes an on-line wafer temperature model in which wafer temperature is predicted based on measurements from the spike and profile thermocouples.

37. A controller unit in accordance with claim 0 wherein the control mode logic circuits include a dynamic control mode logic circuit which controllably supplies power to the heating element based on predicted wafer temperature, and includes an on-line wafer temperature model in which wafer temperature is predicted based on measurements from the spike and profile thermocouples, the dynamic control mode logic circuit including a spike controller which controls power supplied to the heating element in response to measurements by the spike thermocouples, a profile controller which controls the spike controller in response to measurements by the profile thermocouples, and a wafer controller controlling the profile controller in response to the on-line wafer temperature model.

38. A controller unit for controlling a thermal reactor including a heating element powered by a power source, and having profile thermocouples and spike thermocouples, the controller unit comprising:

an on-line model which predicts wafer temperature based on measurements from the spike and profile thermocouples; and

a plurality of selectable control mode logic circuits, the control mode logic circuits including a base control mode logic circuit having a spike controller which controls power supplied to the heating element in response to measurements by the spike thermocouples, and a profile controller which controls the spike controller in response to measurements by the profile thermocouples; a thermal budget control mode logic circuit which measures energy provided to the thermal reactor and controls energy provided to the thermal reactor with respect to desired energy, the thermal budget control mode logic circuit employing the spike controller, and the profile controller, and the thermal budget control mode logic circuit further including a Dt controller controlling the profile controller; and a dynamic control mode logic circuit which controls energy provided to the thermal reactor based on predicted wafer temperature, the dynamic control mode logic circuit employing the spike controller, the profile controller, and the on-line model, the dynamic control mode logic circuit further including a wafer controller in communication with the on-line model and controlling the profile controller.

39. A controller unit in accordance with claim 0 wherein the controllers are respectively derived from off-line models.

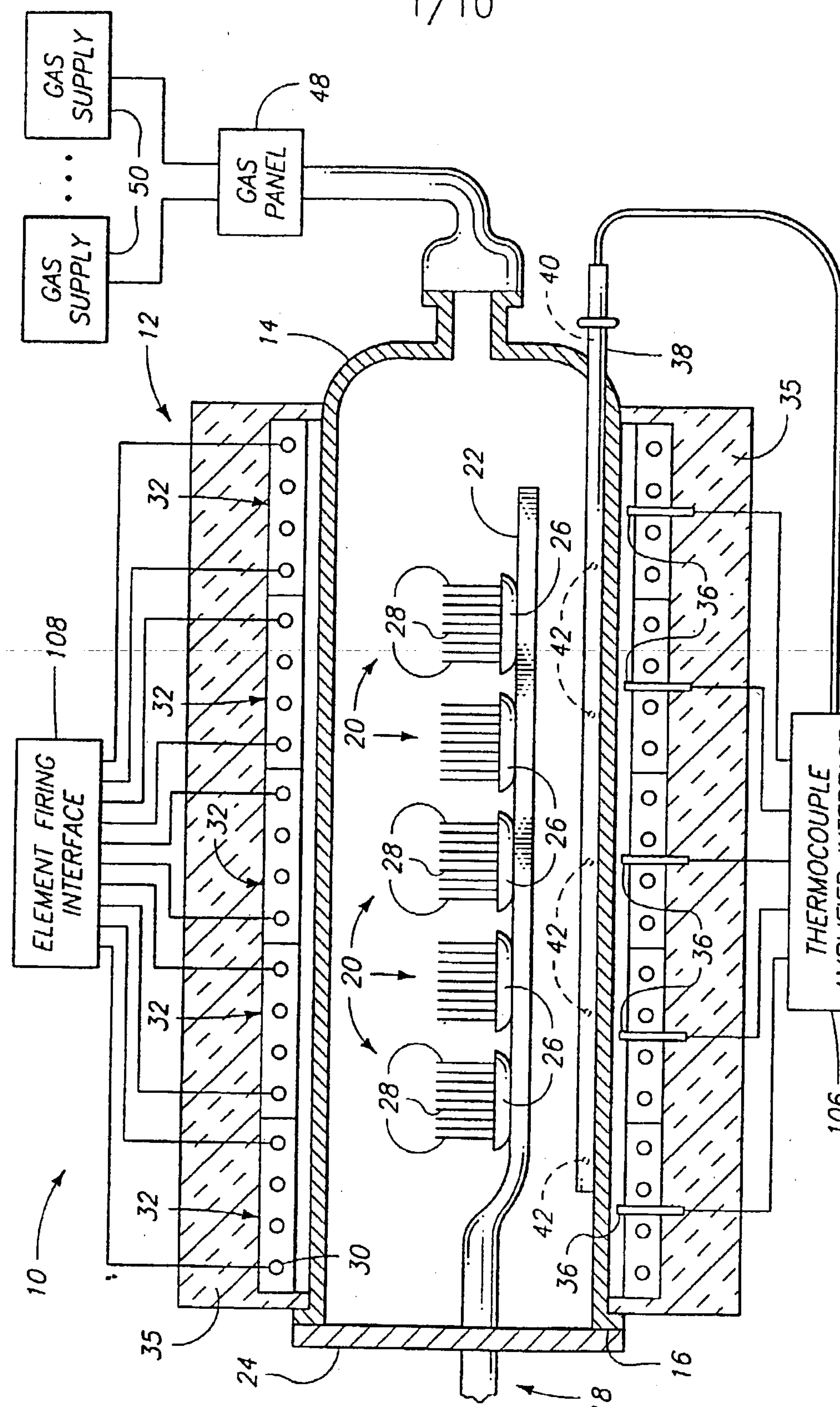
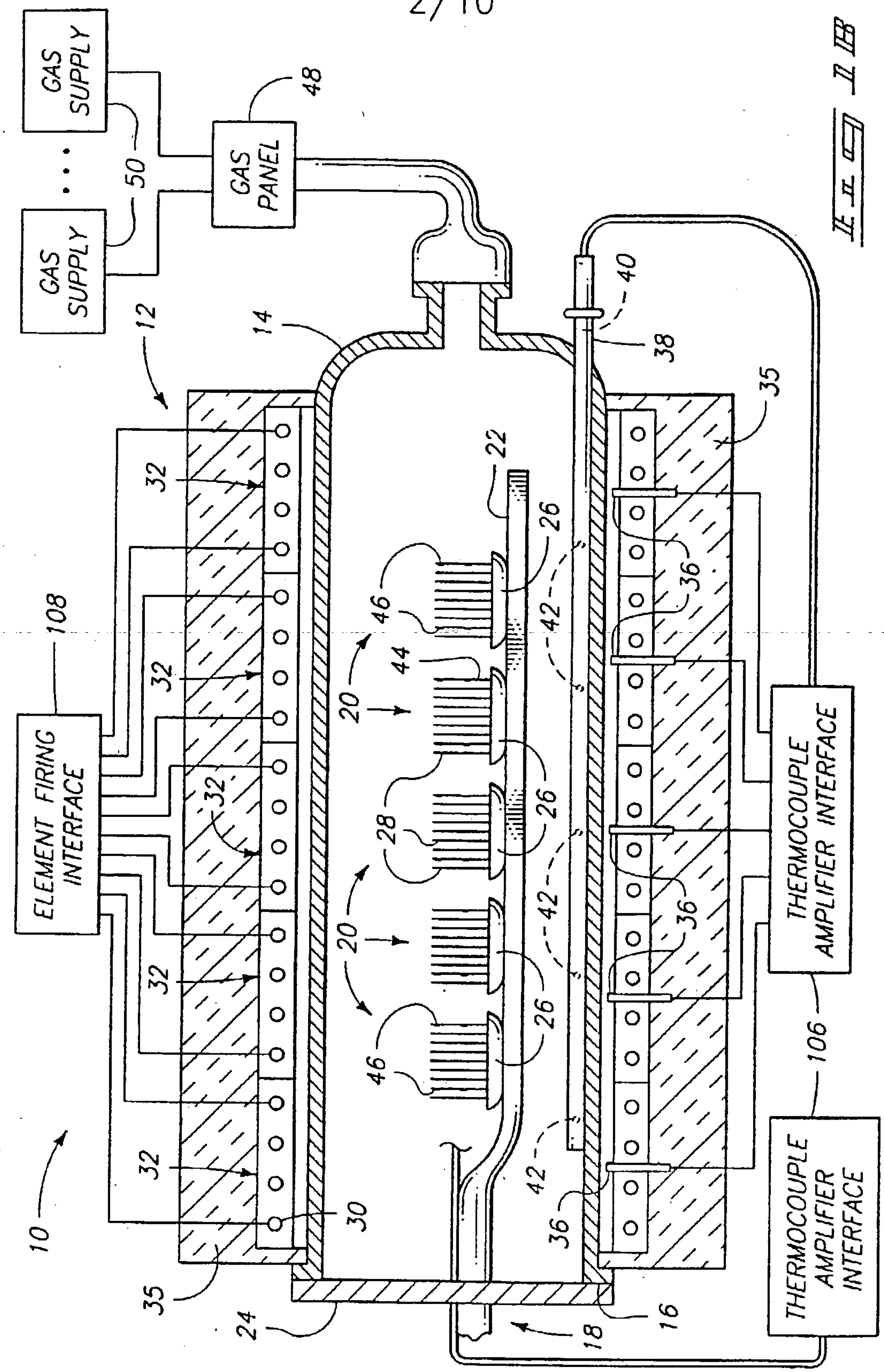
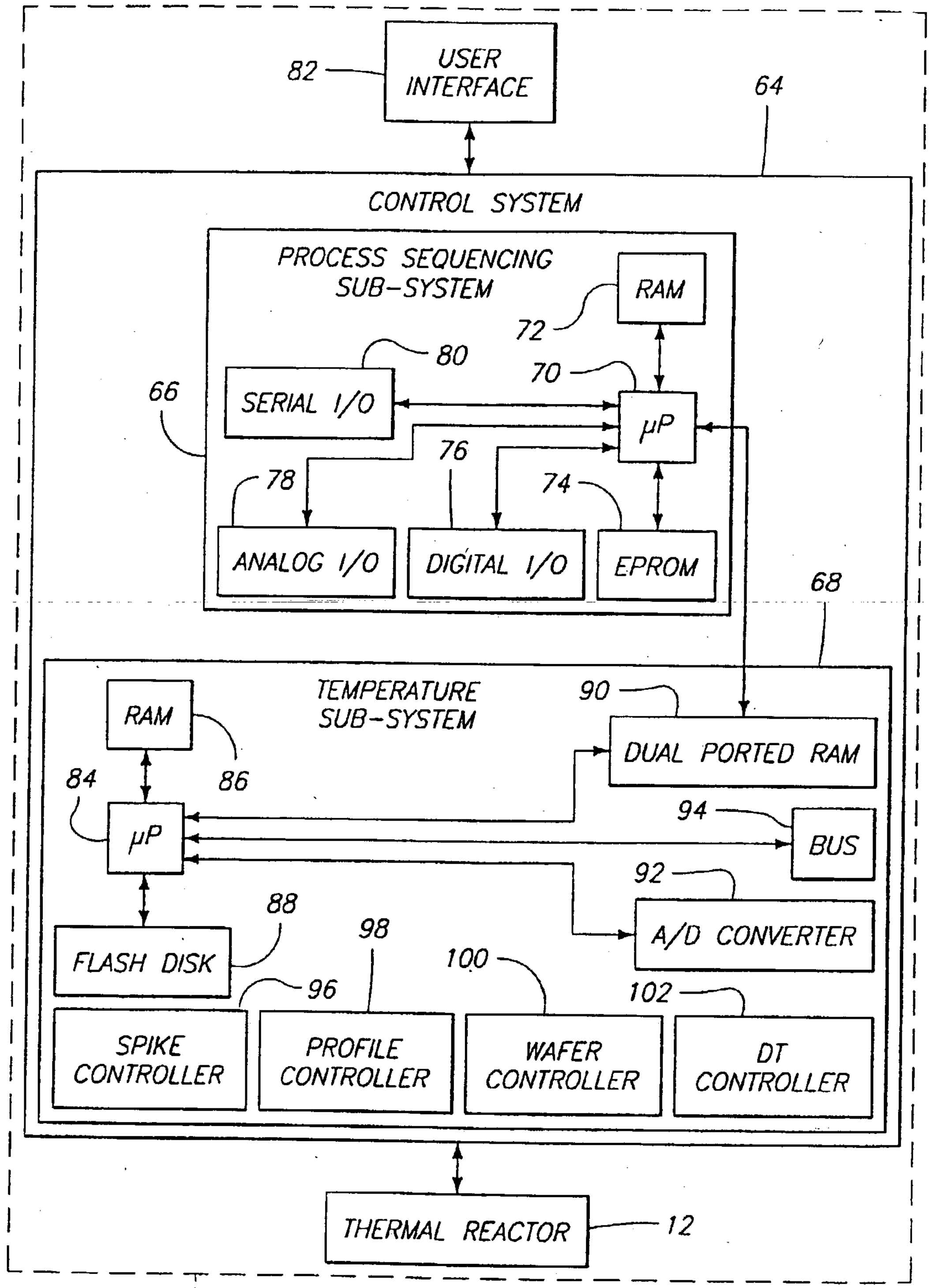

GAS SUPPLY
GAS SUPPLY
50
GAS PANEL
48
12
14
40
38
35
22
26
28
20
32
108
ELEMENT FIRING INTERFACE
42
36
THERMOCOUPLE AMPLIFIER INTERFACE
106
10
30
35
24
18
16

Fig. 1A


GAS SUPPLY
GAS SUPPLY
GAS PANEL
ELEMENT FIRING INTERFACE
THERMOCOUPLE AMPLIFIER INTERFACE
THERMOCOUPLE AMPLIFIER INTERFACE



USER INTERFACE
82
64
CONTROL SYSTEM
PROCESS SEQUENCING SUB-SYSTEM
RAM
72
80
70
66
SERIAL I/O
μP
76
78
74
ANALOG I/O
DIGITAL I/O
EPROM
68
TEMPERATURE SUB-SYSTEM
RAM
90
DUAL PORTED RAM
84
86
94
μP
BUS
92
88
A/D CONVERTER
98
FLASH DISK
100
96
102
SPIKE CONTROLLER
PROFILE CONTROLLER
WAFER CONTROLLER
DT CONTROLLER
THERMAL REACTOR
12
10

Fig 2

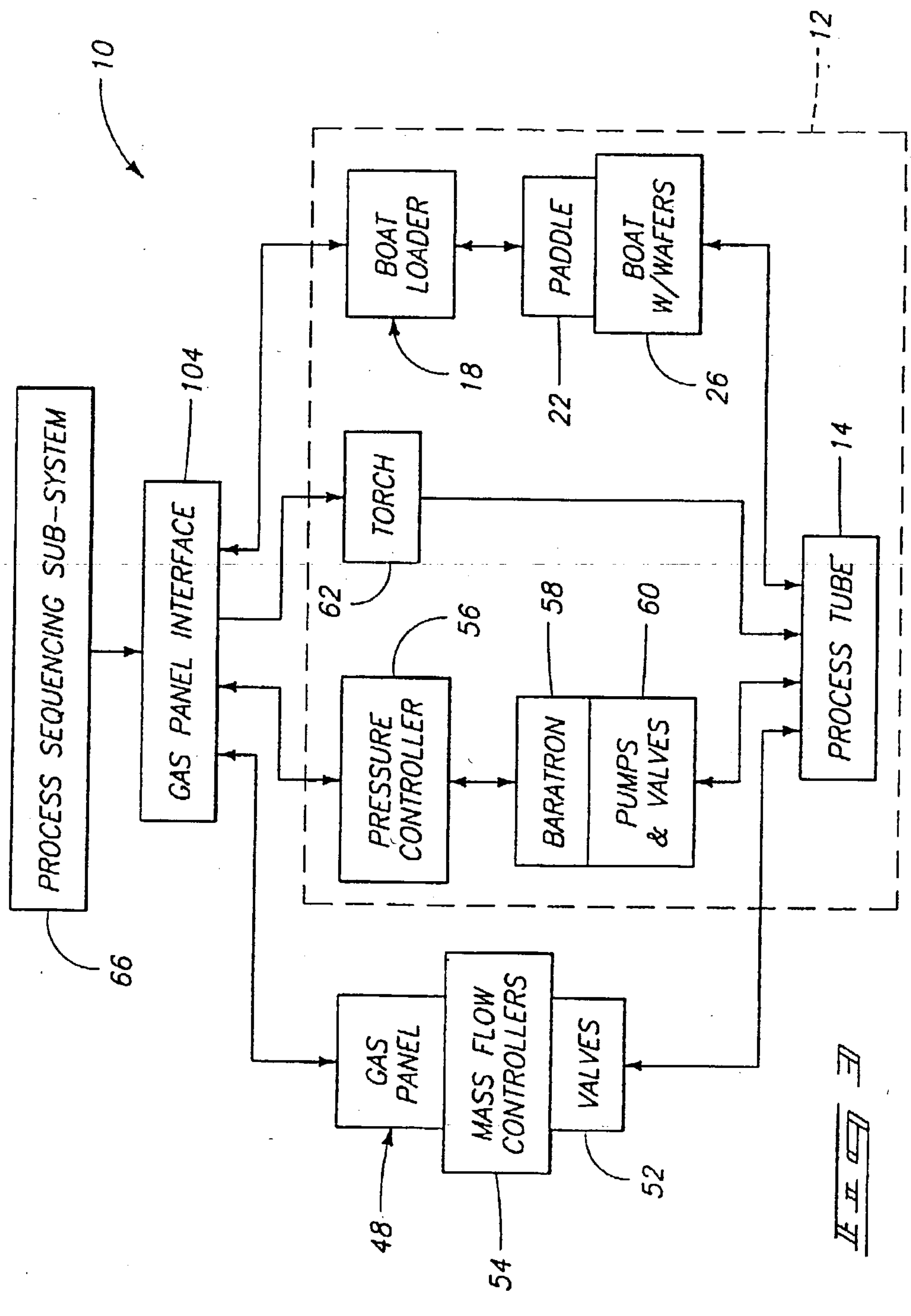

10
12
PROCESS SEQUENCING SUB-SYSTEM
66
GAS PANEL INTERFACE
104
BOAT LOADER
18
PADDLE
22
BOAT W/WAFERS
26
TORCH
62
PROCESS TUBE
14
PRESSURE CONTROLLER
56
BARATRON
58
PUMPS & VALVES
60
GAS PANEL
48
MASS FLOW CONTROLLERS
54
VALVES
52

FIG. 3

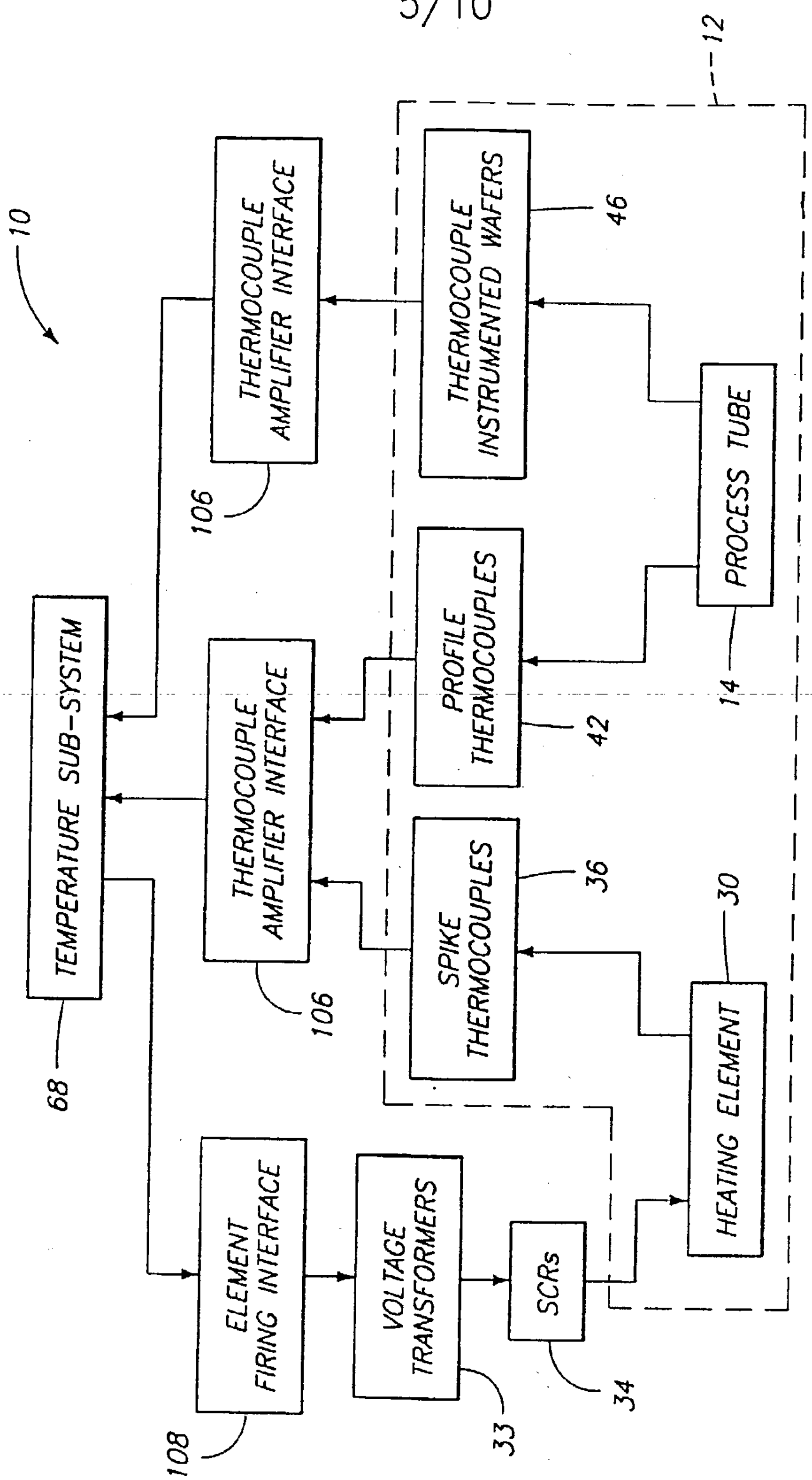

10
12
THERMOCOUPLE AMPLIFIER INTERFACE
106
THERMOCOUPLE INSTRUMENTED WAFERS
46
PROCESS TUBE
14
TEMPERATURE SUB-SYSTEM
68
THERMOCOUPLE AMPLIFIER INTERFACE
106
PROFILE THERMOCOUPLES
42
SPIKE THERMOCOUPLES
36
HEATING ELEMENT
30
ELEMENT FIRING INTERFACE
108
VOLTAGE TRANSFORMERS
33
SCRs
34

FIG. 5

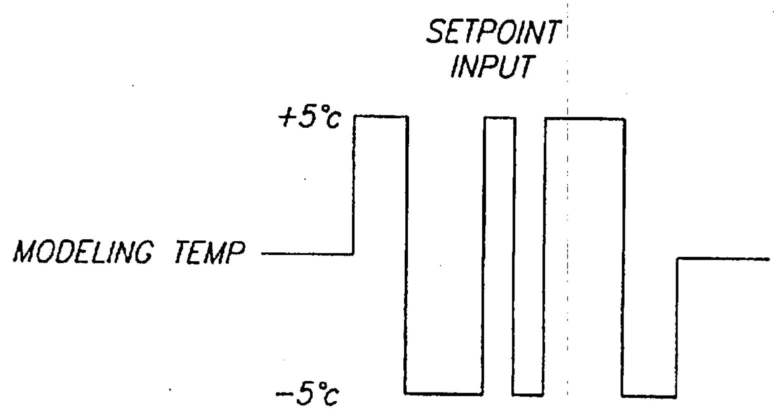

SETPOINT
INPUT
+5°c
MODELING TEMP
-5°c

FIG. 5

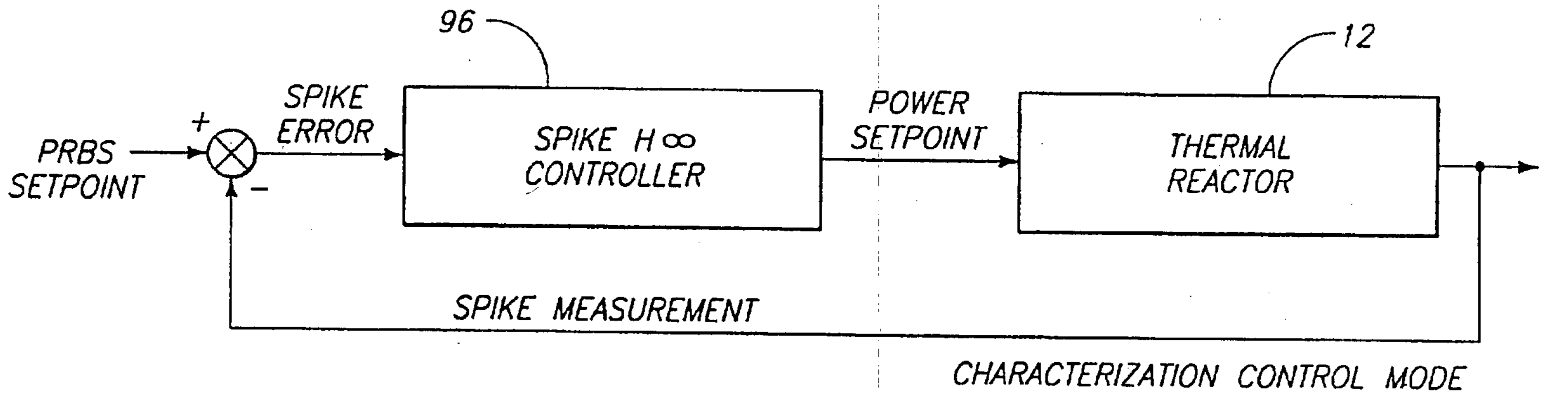

96
12
PRBS
SETPOINT
+
-
SPIKE
ERROR
SPIKE H∞
CONTROLLER
POWER
SETPOINT
THERMAL
REACTOR
SPIKE MEASUREMENT
CHARACTERIZATION CONTROL MODE

FIG. 6

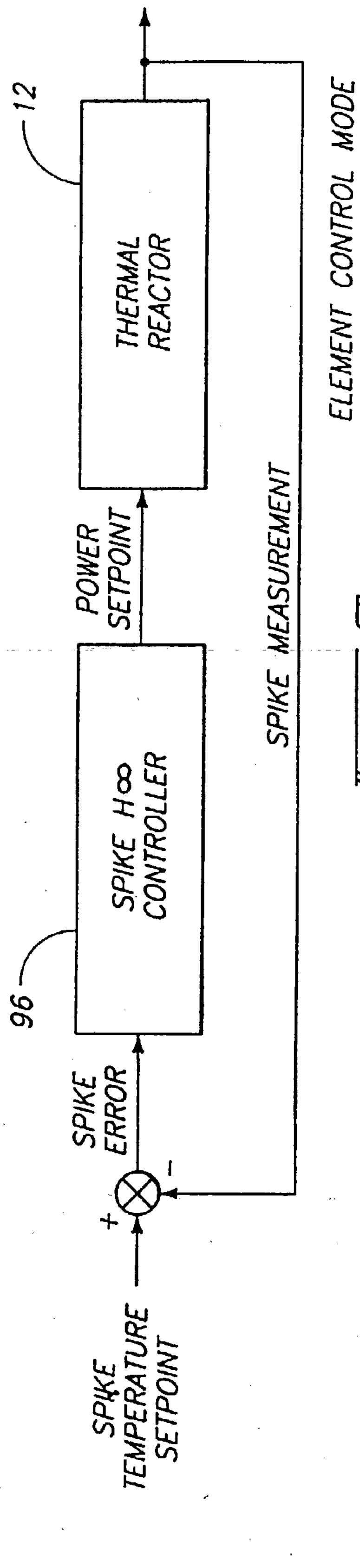

SPIKE TEMPERATURE SETPOINT
+
-
SPIKE ERROR
96
SPIKE H∞ CONTROLLER
POWER SETPOINT
12
THERMAL REACTOR
SPIKE MEASUREMENT
ELEMENT CONTROL MODE

FIG. 7

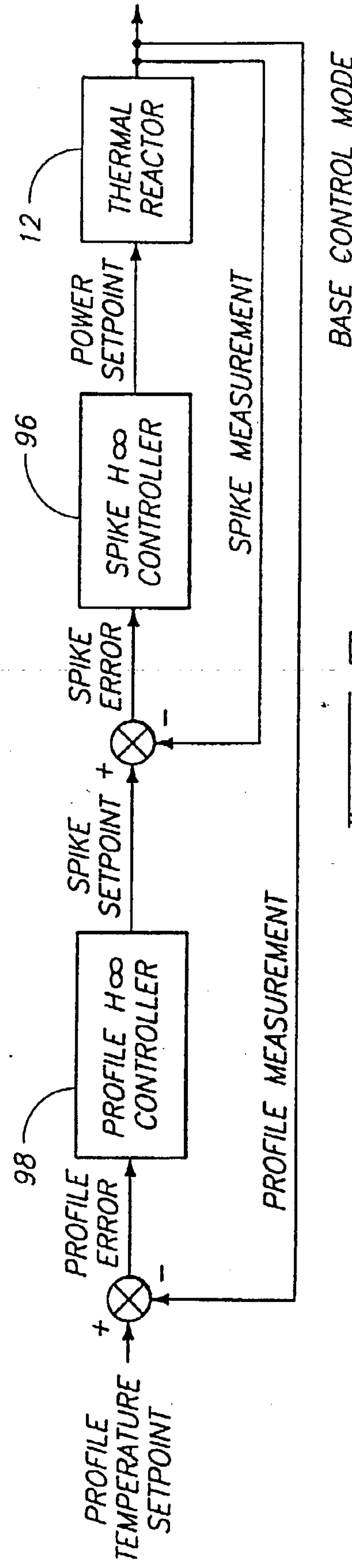

PROFILE TEMPERATURE SETPOINT
+
-
PROFILE ERROR
98
PROFILE H∞ CONTROLLER
SPIKE SETPOINT
+
-
SPIKE ERROR
96
SPIKE H∞ CONTROLLER
POWER SETPOINT
12
THERMAL REACTOR
SPIKE MEASUREMENT
PROFILE MEASUREMENT
BASE CONTROL MODE

FIG. 8

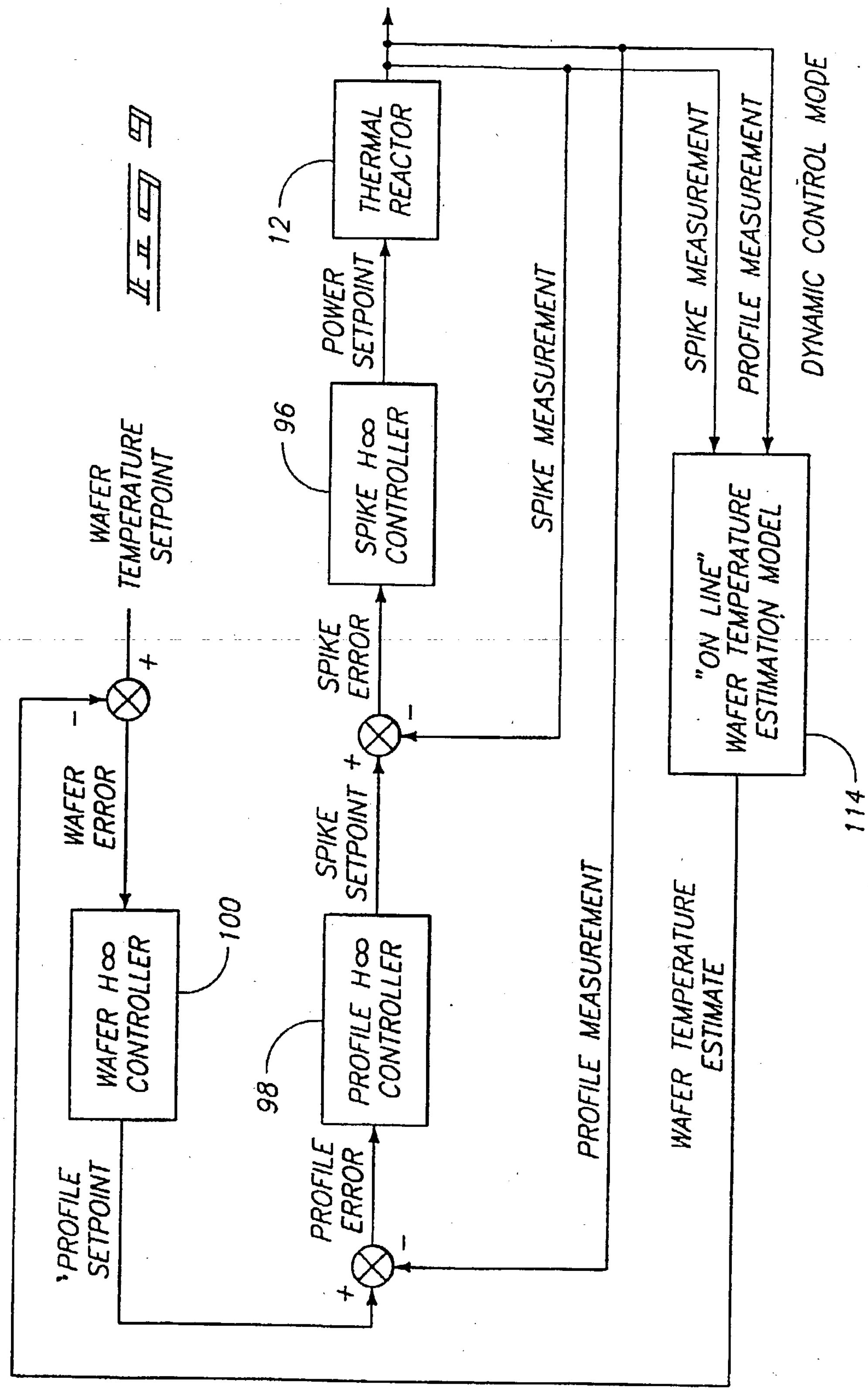

WAFER TEMPERATURE SETPOINT
+
-
WAFER ERROR
WAFER H∞ CONTROLLER
100
PROFILE SETPOINT
+
-
PROFILE ERROR
PROFILE H∞ CONTROLLER
98
SPIKE SETPOINT
+
-
SPIKE ERROR
SPIKE H∞ CONTROLLER
96
POWER SETPOINT
THERMAL REACTOR
12
SPIKE MEASUREMENT
PROFILE MEASUREMENT
SPIKE MEASUREMENT
PROFILE MEASUREMENT
DYNAMIC CONTROL MODE
"ON LINE" WAFER TEMPERATURE ESTIMATION MODEL
114
WAFER TEMPERATURE ESTIMATE

FIG. 9

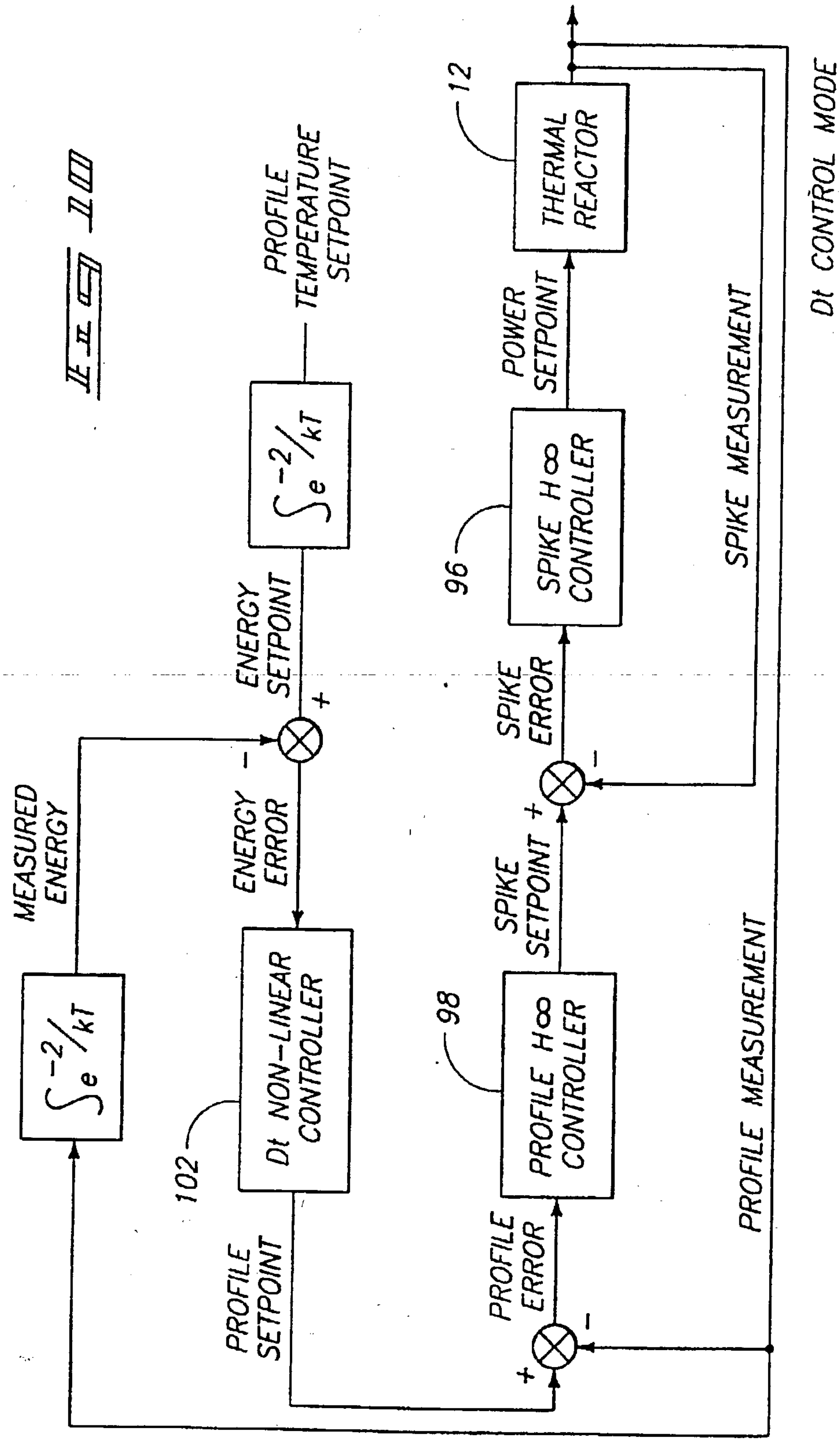

PROFILE TEMPERATURE SETPOINT
$\int e^{-2/kT}$
ENERGY SETPOINT
+
−
MEASURED ENERGY
$\int e^{-2/kT}$
ENERGY ERROR
102
Dt NON-LINEAR CONTROLLER
PROFILE SETPOINT
+
−
PROFILE ERROR
98
PROFILE H∞ CONTROLLER
SPIKE SETPOINT
+
−
SPIKE ERROR
96
SPIKE H∞ CONTROLLER
POWER SETPOINT
12
THERMAL REACTOR
SPIKE MEASUREMENT
PROFILE MEASUREMENT
Dt CONTROL MODE

FIG. 10

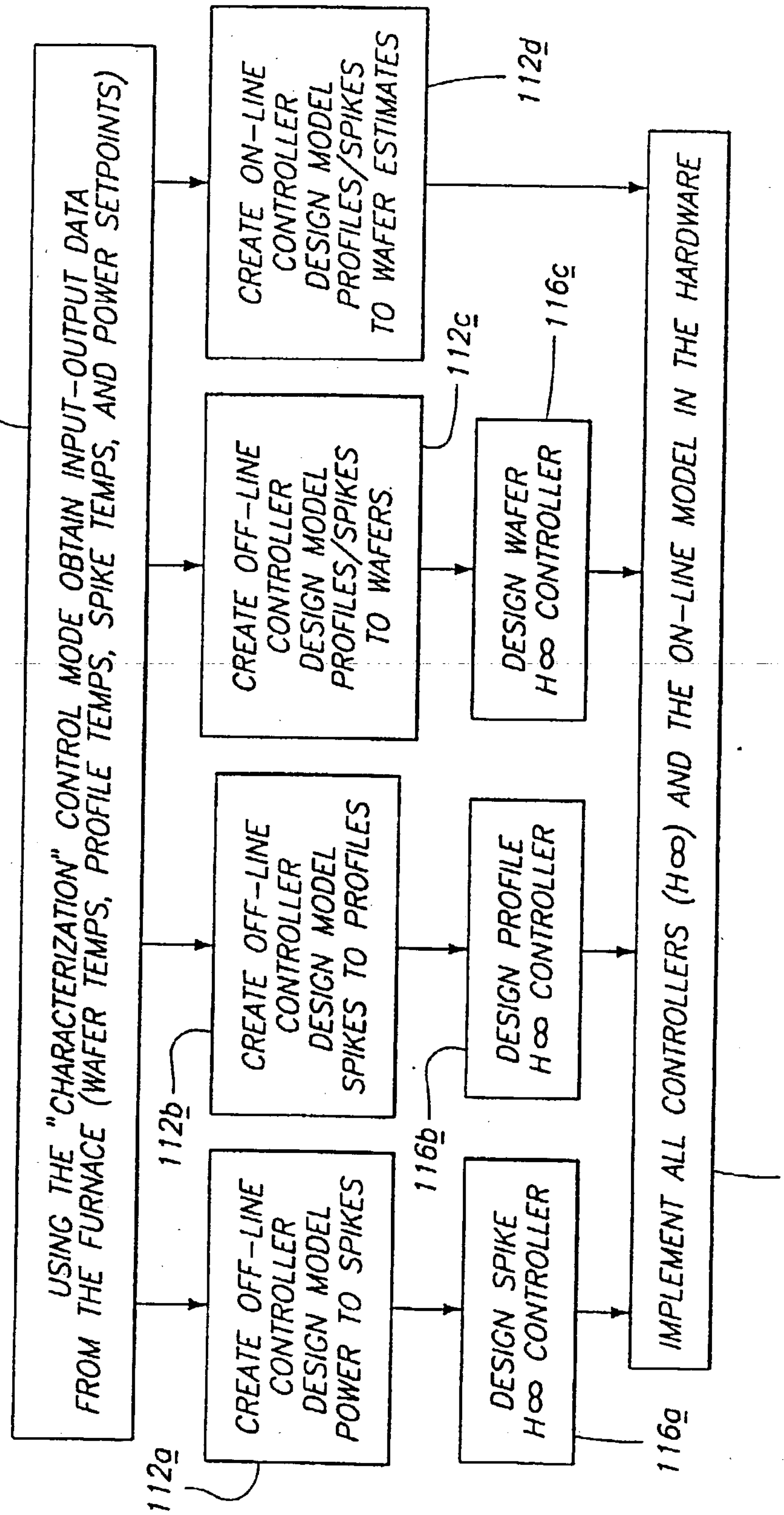

110
USING THE "CHARACTERIZATION" CONTROL MODE OBTAIN INPUT-OUTPUT DATA FROM THE FURNACE (WAFER TEMPS, PROFILE TEMPS, SPIKE TEMPS, AND POWER SETPOINTS)
112a
CREATE OFF-LINE CONTROLLER DESIGN MODEL POWER TO SPIKES
112b
CREATE OFF-LINE CONTROLLER DESIGN MODEL SPIKES TO PROFILES
112c
CREATE OFF-LINE CONTROLLER DESIGN MODEL PROFILES/SPIKES TO WAFERS
112d
CREATE ON-LINE CONTROLLER DESIGN MODEL PROFILES/SPIKES TO WAFER ESTIMATES
116a
DESIGN SPIKE H∞ CONTROLLER
116b
DESIGN PROFILE H∞ CONTROLLER
116c
DESIGN WAFER H∞ CONTROLLER
118
IMPLEMENT ALL CONTROLLERS (H∞) AND THE ON-LINE MODEL IN THE HARDWARE

Fig. 11

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US98/01076

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :HO5B 1/02 ,C23C 1454
US CL :Please See Extra Sheet.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 392/416; 219/497,483,486;
118/725

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

156/345;
219/501,485, 494,505

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS, Japanese Patent Abstracts

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US,5,517,594 A (SHAH ET AL) 14 MAY 1996, SEE ENTIRE DOCUMENT.	1-39
Y	US 5,099,442 A (FURUTA et al) 24 March 1992, SEE ENTIRE DOCUMENT.	1-39
A	US 5,258,601 A (TAKANO) 02 NOVEMBER 1993 , SEE ENTIRE DOCUMENT.	1-39
A	US 4,937,434 A (NAKAO) 26 JUNE 1990, SEE ENTIRE DOCUMENT .	1-39
A	US 4,761,538 A (CHIBA ET AL) 02 AUGUST 1988, SEE ENTIRE DOCUMENT	1-39

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
06 APRIL 1998	07 JUL 1998

Name and mailing address of the ISA/US	Authorized officer
Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231	MARK H. PASCHALL
Facsimile No. (703) 305-3230	Telephone No. (703) 308-1642

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US98/01076

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This international report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☒ Claims Nos.: 2-6,8-12,14-17,19-22,26-30,32-37,39
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

Note that all of these claims depend on claim 0 , and therefore are unsearchable.

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US98/01076

A. CLASSIFICATION OF SUBJECT MATTER:
US CL :

392/416; 219/497,483,486;
118/725